

We claim:

- 1 1. An apparatus comprising:
 - 2 first and second execution cores to operate in an FRC mode;
 - 3 an FRC check unit to compare results from the first and second execution cores
 - 4 and to store at least one result and a status to indicate if the results match;
 - 5 an error check unit to assert a signal to the FRC checker if a recoverable error is
 - 6 detected in the first or second execution cores; and
 - 7 a timer to trigger an FRC recovery routine if the status indicates the results do not
 - 8 match and the error check unit does not assert the signal within a specified interval.
- 9 2. The apparatus of claim 1, wherein the FRC checker stores a result from the master
- 10 execution core and discards the result from the slave execution core.
- 11 3. The apparatus of claim 2, wherein the FRC checker stalls the slave execution core if the
- 12 status indicates the results do not match and triggers a countdown to the specified interval.
- 13 4. The apparatus of claim 4, wherein the specified interval represents a time for a
- 14 recoverable error to be signaled to the error detector.
- 15 5. The apparatus of claim 1, wherein the FRC check unit includes a multiple entry buffer to
- 16 store results and status indicators for multiple.

1 6. The apparatus of claim 2, wherein a number of entries for the buffer is selected to
2 determined by a largest number of clock cycle to propagate an error signal to the error detector.

1 7. The apparatus of claim 1, wherein the FRC check unit includes a buffer to store results
2 from the first and second execution cores and their status.

1 8. The apparatus of claim 7, wherein the recovery routine reads an uncorrupted result from
2 an appropriate entry of the buffer if the recoverable error is detected within the specified interval.

1 9. An system comprising:
2 first and second execution cores to operate in an FRC mode;
3 an FRC checker to compare results from the first and second execution cores and
4 to trigger a countdown interval if the results do not match; and
5 an error detector to monitor error signals during the countdown interval and to
6 disable the FRC checker if a recoverable error is detected before the countdown interval
7 expires.

1 10. The system of claim 9, wherein the FRC checker includes a buffer to temporarily store
2 results from at least one of the first and second execution cores.

1 11. The system of claim 9, wherein the FRC checker stalls one of the first and second
2 execution cores if the results do not match.

1 12. The system of claim 9, further comprising a recovery unit to recover uncorrupted results
2 from the first or second execution core, responsive to the error detector detecting a recoverable
3 error.

1 13. The system of claim 12, further comprising a reset unit to reset the system, responsive to
2 the FRC checker indicating an FRC error.

1 14. The system of claim 13, wherein the FRC checker indicates an FRC error if results from
2 the first and second execution pipelines do not match and the FRC checker is not disabled before
3 the countdown interval expires.

1 15. The system of claim 13, further comprising a memory device in which a recovery routine
2 and a reset routine are stored.

1 16. The system of claim 15, wherein the recovery unit and the reset unit include pointers to
2 the recovery routine and the reset routine, respectively.

1 17. A method comprising:

2 comparing results from a first and second execution core to detect an FRC error;
3 if the results do not match, setting a first flag and initiating a countdown interval;
4 monitoring an error signal for a recoverable error; and
5 initiating a recovery routine if the error signal is asserted before the countdown
6 interval expires.

1 18. The method of claim 17, further comprising:

storing a result from at least one of the first and second execution cores; and
initiating a transaction to a shared resource if the first flag is not set.

19. The method of claim 18, further comprising initiating a reset routine if the error signal is
not asserted before the countdown interval expires.

1 20. The method of claim 17, further comprising:

2 stalling one of the first and second execution cores if the first flag is set; and
3 continuing to monitor the error signal from the stalled execution core.